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Book Announcement: ***Life-Cycle Forecasting, Mitigation Assessment and Obsolescence Strategies***

Anomalous Radiation Effects in Fully-Depleted SOI MOSFETs Fabricated on SIMOX

Ying Li, Guofu Niu, John D. Cressler, Jagdish Patel, Cheryl J. Marshall, Paul W. Marshall, Hak S. Kim, Robert A. Reed, and Michael J. Palmer

Abstract:

We investigate the proton tolerance of fully-depleted SOI MOSFETs with H-gate and regular-gate structural configurations. For the front-gate characteristics, the H-gate does not show the edge leakage observed in the regular-gate transistor. An anomalous kink in the back-gate linear ID-VGS characteristics of the fully-depleted SOI nFETs has been observed at high radiation doses. This kink is attributed to charged traps generated in the bandgap at the buried oxide/silicon film interface during irradiation. Extensive 2-D simulations with MEDICI were used to understand the physical origin of this kink. We also report unusual self-annealing effects in the devices when they are cooled to liquid nitrogen temperature.

The entire report may be viewed at the NEPP Web Site:
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Assessing the Impact of the Space Radiation Environment on Parametric Degradation and Single Event Transients in Optocouplers

R.A. Reed, C. Poivey, P.W. Marshall, K.A. LaBel, C.J. Marshall, S. Kniffin, J.L. Barth, and C. Seidleck

Abstract:

Assessing the risk of using optocouplers in satellite applications offers challenges that incorporate those of commercial off-the-shelf devices compounded by hybrid module construction techniques. We discuss approaches for estimating this risk. In the process, we benchmark our estimates for proton and heavy ion induced single event transient rate estimates with recent flight data from the Terra mission. For parametric degradation, we discuss a method for acquiring test data and mapping it into an estimation approach that captures all the important variables of circuit application, environment, damage energy dependence, complex response to TID and displacement effects, temperature, and annealing.

The entire report may be viewed at the NEPP Web Site:
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Characterization of Transient Error Cross Sections in High Speed Commercial Fiber Optic Data Links

**Cheryl J. Marshall, Paul W. Marshall2, Martin A. Carts,
Robert Reed, Steve Baier, and Ken LaBel**

Abstract:

This paper presents data on the single event transient (SET) response of several high speed commercial fiber optic links (FOLs). We show that commercial-grade technologies may be robust to SET in the natural space environment encountered in many satellite missions even for data rates in the 1 Gbps regime. In addition to characterizing the error cross section as a function of optical power and data rate, the angular dependence of the SET behavior is also quantified as a function of optical power. Note that receiver angular response has some similarity to behavior observed in optocoupler technology and must be quantified for accurate predictions of on-orbit link error rates [1,2].

The entire report may be viewed at the NEPP Web Site:
Click Here to View

Development of a Test Methodology for Single Event Transients (SET) in Linear Devices

**Christian Poivey, James W. Howard, Jr., Steve Buchner, Kenneth A. LaBel,
James D. Forney, Hak S. Kim, and Arheindal Assad**

Abstract:

We present SET test data on linear devices under many operational conditions in an attempt to understand the SET generation and characteristics. This is done in an attempt to define a low–cost, conservative test methodology to characterize these effects.

The entire report may be viewed at the NEPP Web Site:
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The Effects of Proton Irradiation on SiGe:C HBTs

Shiming Zhang, Guofu Niu, John D. Cressler, Hans-Joerg Osten, Dieter Knoll, Cheryl J. Marshall, Paul W. Marshall, Hak S. Kim, and Robert A. Reed

Abstract:

The effects of 63MeV proton irradiation on SiGe:C HBTs are reported for the first time. The dc characteristics and neutral base recombination of these SiGe:C HBTs are investigated for proton fluences up to 5×1013 p/cm2. A comparison is made with SiGe HBTs fabricated in the same technology. Despite the fact that these SiGe:C HBTs degrade significantly during proton exposure, there is no indication that the carbon doping has any significant impact on the radiation response.

The entire report may be viewed at the NEPP Web Site:
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Modeling of Single Event Effects in Circuit-Hardened High-Speed SiGe HBT Logic

Guofu Niu, Ramkumar Krithivasan, John D. Cressler, Paul Marshall, Cheryl Marshall, Robert Reed, and David L. Harame

Abstract:

This paper presents SEE modeling results of circuit-hardened SiGe HBT logic circuits. A simple equivalent circuit is proposed to model the ion-induced currents at all of the terminals, including the p-type substrate. The SEE sensitivity of a D flip-flop was simulated using the proposed equivalent circuit. The simulation results are qualitatively consistent with earlier SEE testing results. The circuit upset is shown to be independent of the number of active paths. Considerable charge collection occurs through the reverse biased n-collector/p-substrate junction, regardless of the status of the emitter steering current, resulting in circuit upset through the commonly connected load resistor. A heavily doped substrate is shown to be beneficial for SEE.

The entire report may be viewed at the NEPP Web Site:
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1/f Noise in Proton Irradiated SiGe HBTs

Zhenrong Jin, Guofu Niu, John D. Cressler, Cheryl J. Marshall, Paul W. Marshall, Hak S. Kim, Robert Reed, and David L. Harame

Abstract:

This paper investigates the impact of proton irradiation on the 1/f noise in UHV/CVD SiGe HBTs. The relative degradation of 1/f noise shows a strong dependence on device geometry. Both the geometry dependence and the bias dependence of 1/f noise change significantly after exposure to 2 x 10^3 p/cm^2 protons. "An expression describing the 1/f noise is derived, and used to explain the experimental observations."

The entire report may be viewed at the NEPP Web Site:
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Recent Radiation Damage and Single Event Effect Results for Candidate Spacecraft Electronics

Martha V. O'Bryan, Kenneth A. LaBel, Robert A. Reed, Ray L. Ladbury, James W. Howard Jr., Stephen P. Buchner, Janet L. Barth, Scott D. Kniffin, Christina M. Seidleck, Cheryl J. Marshall, Paul W. Marshall, Hak S. Kim, Donald K. Hawkins, Martin A. Carts, James D. Forney, Anthony B. Sanders, Stephen R. Cox, Curtis J. Dunsmore, and Christopher Palor

Abstract:

We present data on the vulnerability of a variety of candidate spacecraft electronics to proton and heavy ion induced single event effects and proton-induced damage. Devices tested include optoelectronics, digital, analog, linear bipolar, hybrid devices, Analog-to-Digital Converters (ADCs), Digital-to-Analog Converters (DACs), and DC-DC converters, among others.

The entire report may be viewed at the NEPP Web Site:
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Total Dose and Single Event Effects Testing of the Intel Pentium III (P3) and AMD K7 Microprocessors

James W. Howard Jr., Martin A. Carts, Ronald Stattel, Charles E. Rogers, Timothy L. Irwin, Curtis Dunsmore, J. Anthony Sciarini and Kenneth A. LaBel

Abstract:

To understand the radiation sensitivity and radiation response, Intel Pentium III and AMD K7 microprocessors were tested for total ionizing dose and single event effects. The processors have been found to be extremely tolerant to total ionizing dose and no radiation induced latchups have been observed with protons or heavy ions to an LET of approximately 15 MeV-cm2/mg. Single event upset and functional interrupts have been observed with both protons and heavy ions.

The complete report is available for viewing at the NEPP Web Site:

The entire report may be viewed at the NEPP Web Site:
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Special Events

Third Annual NEPP Workshop Aftermath

The Third Annual NEPP Workshop was held April 30-May 2 in Houston, Texas, across from Johnson Space Center. 100 people attendend with approximately half from NASA, a few from other Government agencies, and the remainder from industry. Most NASA Centers sent at least one attendee. Session topics included High Temperature Environments, Low Temperature Environments, NASA-Langley Macro-Fiber Composites (LaRC-MFC Technology), Innovative Qualification and Test Methods, Radiation Hardness Assurance, Optoelectronics, MicroElectroMechanical Systems (MEMS) and MicroOptoElectroMechanical Systems (MOEMS), Advanced Sensors, Radiation Effects on Technology, Parts and Packaging Reliability, and Commercial Off-The-Shelf Plastic Encapsulated Microcircuits (COTS PEMS).

Biographies of the workshop participants and abstracts of their presentations can be found in the NEPP Workshop Program Guide, which is available by **clicking here.**

CALCE Press

Lifetime RC Time Delay of On-Chip Copper Interconnect

Ming Sun, *Associate Member, IEEE*, Michael G. Pecht, *Fellow, IEEE*, and David Barbe, *Fellow, IEEE*

***Abstract*—Increasing resistance and RC time delay induced by an oxidation in a copper line during its lifetime may limit copper-based metallization for technologies with critical dimension. Based on the mechanisms of resistance, constriction resistance and material diffusion, two dynamic models to access lifetime behavior of resistance and RC time delay were developed and discussed. These models also provide a means to gain insight into the correlation between the resistance and RC time delay of copper interconnect and such key variables as feature dimension, operating condition, and oxidation.**

***Index Terms*—Constriction resistance, copper interconnect, diffusion, oxidation, RC delay.**

I. Introduction

THE SWITCH to copper interconnects from aluminum interconnects provides several advantages, such as chip speed increment, power dissipation minimization and manufacturing cost reduction due to an increase in circuitry density.

However, copper technology has also its specific problems. Because copper surfaces are highly electrochemically active and do not form a natural protective layer, so they corrode and oxidize easily. Copper reacts with oxidizing agents, silicon, silicides, and other metals commonly used for ultralarge-scale integrated circuit metallization and packaging at relatively low temperatures [1].

The problems of copper's penetration into the dielectrics, oxidation and reaction with silicon and other metals can be overcome with the use of barrier layers, for example titanium nitride, tantalum nitride and tantalum silicon nitride by chemical vapor deposition (CVD) or physical vapor deposition (PVD) [2]. However, these barriers may create other reliability hazards due to process-induced defects or voids on barrier layers, defects induced by chemical-mechanical polishing (CMP), and stress effects on the metal integrity during thermal processing and under electromigration stressing [3].

These defects induced during processing could result in the formation of oxidation or corrosion pits in the copper interconnects. Furthermore, the insulating pits grow during the lifetime, induce an additional resistance into the interconnects which is called, constriction resistance caused by the limitation of current flow in the vicinity of pit area [3], [4]. Constriction resistance is the term used to describe a localized resistance increase due to the reduction of conduction area in cross section when current lines of flow are bent together through narrow area. This additional resistance makes the RC (resistance $\times$ capacitance) time delay of interconnects increase and the device performance decrease.

Previous experimental studies of copper interconnects show that the increase in resistance of the copper interconnect is due to the growth of copper oxides or corrosion products [5]. Resistance in signal lines increases, as cross-sectional area reduces, can be several ohms per centimeter length in the thin-film copper interconnect. As critical dimensions of interconnects are being scaled down in developing a next generation of copper interconnect for ULSI applications, obviously, the lifetime tendencies of resistance and RC time delay become two of major concerns. This paper presents a dynamic approach to describe the lifetime variation of resistance, RC time delay and physical relations with key operating parameters.

II. Interconnect Structure

A. Bare Line

In order to model the shrinkage of a bare copper line at cross section in terms of mathematics model, the cross section has been assumed to be uniform along the copper interconnect. Figs. 1 and 2 schematically show views of the shrinkage of copper line with the growth of oxidized region and distribution of copper concentration in the oxidized region of copper interconnect. Obviously, as it is one-dimensional (1-D) diffusion of copper and growth of oxide film, it can be solved by 1-D diffusion equation.

Let us consider first, the period $0 \leq t \leq t_p$ of nonstationary diffusion, assuming a concentration is independent of diffusion coefficient D ($\mathrm{cm^2 s^{-1}}$) of copper in the oxidized region. Here, t_p is defined as the time that, the whole cross section of the copper line has been oxidized. The unit chosen for the concentration of element (C) is not specified since the formulas for diffusion are independent of the special choice. We therefore choose mass, number of gram molecules (moles), number of molecules, or whatever unit may seem to be most convenient in the case under consideration.

After time t, the oxidized region extends from Z' to Z''. Copper diffusion in this region obeys the following differential equation (Fick's Second Law):

$$\frac{\partial C}{\partial t} = D_{\mathrm{Cu}} \frac{\partial^2 C}{\partial Z^2}, \quad \text{for } Z' < Z < Z''. \tag{1}$$

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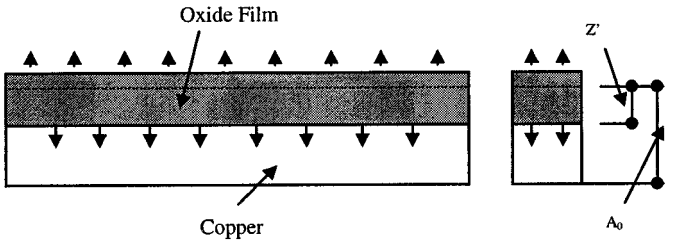


Fig. 1. Copper interconnect shrinks as the oxide film grows.

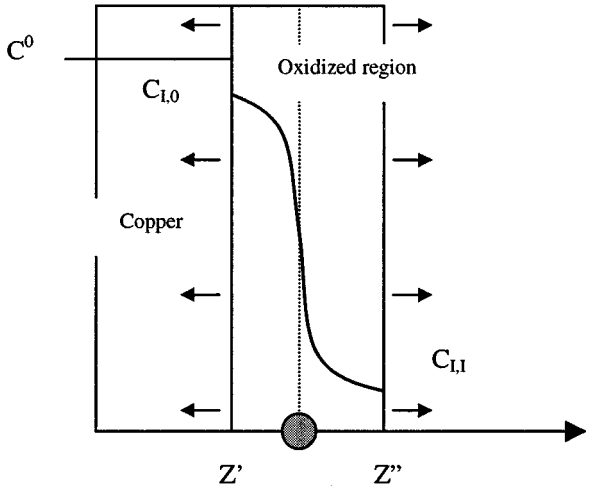


Fig. 2. Copper concentration in copper ($Z < Z'$), in oxidized or corroded region of copper line ($Z' < Z < Z''$), and in silicon dioxide ($Z > Z''$) at $t > 0$.

Initial boundary conditions, $(t = 0)$ are:

$$C = C^{\circ}, \quad \text{for } Z < 0 \tag{2}$$

and

$$C = 0, \quad \text{for } Z > 0. \tag{3}$$

Following [6], assume tentatively that the plane of discontinuity is shifted proportionally with $\sqrt{t}$, i.e., (See Appendix A for the derivation),

$$Z' = \gamma' 2\sqrt{D_{\mathrm{Cu}} t} \tag{4}$$

$$Z'' = \gamma'' 2\sqrt{D_{\mathrm{Cu}} t} \tag{5}$$

where γ', γ'' are two dimensionless parameters.

A particular solution [6] of (1) is

$$C = A - \mathrm{Berf}\left[\frac{Z}{2\sqrt{D_{\mathrm{Cu}} t}}\right] \quad \text{for } Z' < Z < Z''. \tag{6}$$

Similar to the above analysis, we can have another one dimensional diffusion equation for oxidizing agent, such as oxygen. Therefore, the boundary growth inward can also be expressed as (7) after performing the same procedure as above,

$$Z' = 2\gamma' \sqrt{Dt} \tag{7}$$

where

$$D = D_0 e^{-\frac{Q_a}{RT_a}} \tag{8}$$

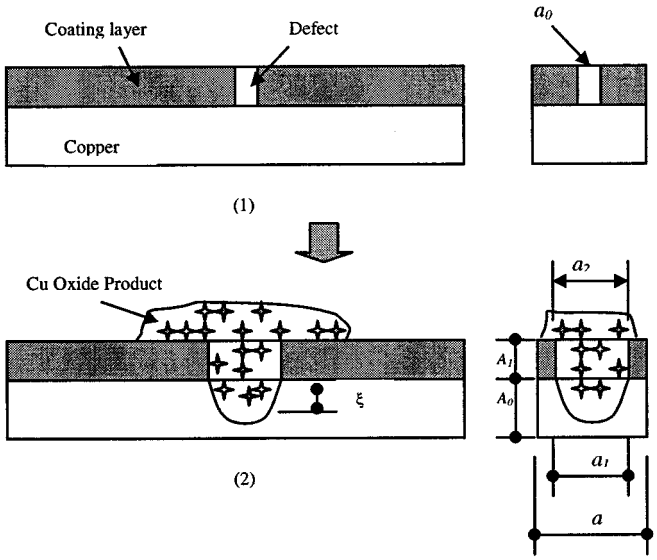


Fig. 3. The pitting process of coated copper interconnects during oxidizing, (1) initial imperfection or pore and (2) oxidized region in the copper line.

where D_0 is the frequency factor for the oxidizing agent, Q_a the activation energy of oxidizing agent through the copper oxide product, and R universal gas constant. T_a is the absolute temperature of the oxidized region.

B. Localized Shrinkage

A localized reduction in the cross section of the coated copper interconnect is a result of the formation of pits due to extremely localized attack of oxidizing agent at the imperfections of barrier and plating or coating layer. These pits may be small in the initial stage and grow continuously during the lifetime of copper interconnect. The consecutive growth of these pits, or reduction of the conductive area of copper line makes it more difficult for a current to flow in this region of copper line, and thus results in an additional electrical resistance in this region, called the electrical constriction resistance [4].

Pits can develop and grow on the copper line surface at imperfections of barrier and coating or plating layers. Fig. 3 schematically shows an example of pitting the coated copper line during an oxidizing process. The conductive region of the copper line decreases gradually as copper oxide products grow.

Following the reasoning used by *Tompkins* and *Crank* [6]–[8], based on the mechanism of oxidizing agent diffusion, the depth ξ of the oxidation zone is a parabolic function of the time if diffusion control prevails. Then we may let

$$\xi = \frac{a_1}{2} = \gamma\sqrt{Dt} \tag{9}$$

where a_1 is the diameter of the hemisphere that is assumed to express the oxidized region in the copper, γ is a dimensionless parameter which can be calculated in terms of the oxidizing agent concentration at the interfaces and D is the diffusion coefficient of oxidizing agent, which has the form of (8).

Using the copper line with noble plating as an example at following derivation (similarly, derivations for copper line with

coating or barrier layers could be conducted), assume that the initial area of the conductive cross section, S_0, is

$$S_0 = aA_1 + aA_0 - a_0A_1, \tag{10}$$

while the area of the conductive cross section after the oxidizing process, S, is

$$S = (a - a_2)A_1 + aA_0 - \frac{1}{8}\pi a_1^2. \tag{11}$$

Assuming that the defect diameter at the plating layer increases from a_0 to a_2, a_2 is equal to a_1 due to a mechanical damage accompanied with the growth of copper oxide region during the oxidizing process and substituting (8) and (9) into (11), we have

$$\begin{aligned} S &= (a - a_1)A_1 + aA_0 - \frac{1}{8}\pi a_1^2 \\ &= a(A_0 + A_1) - 2\gamma A_1 t^{\frac{1}{2}} D_0^{\frac{1}{2}} e^{-\frac{Q_a}{2RT_a}} - \frac{1}{2}\pi\gamma^2 t D_0 e^{-\frac{Q_a}{RT_a}}. \end{aligned} \tag{12}$$

Thus, the area of the conductive cross section is a function of time, temperature, activation energy of diffusion of oxidizing agent in the oxidizing region and concentration of oxidizing agent. In general, the above (12) can be used to estimate the reduction of the conductive cross section during the lifetime application of a copper interconnect. However, with regard to the fact that coating layer is several orders of magnitude thinner than the copper base layer, the net increase in the defect diameter of the coating layer can be neglected assuming $a_2 = a_0$, in order to simplify the model of the lifetime resistance to be derived in the next section. Thus, (12) becomes

$$\begin{aligned} S &= (a - a_0)A_1 + aA_0 - \frac{1}{8}\pi a_1^2 \\ &= a(A_0 + A_1) - a_0A_1 - \frac{1}{2}\pi\gamma^2 t D_0 e^{-\frac{Q_a}{RT_a}}. \end{aligned} \tag{13}$$

III. Lifetime Resistance and RC Time Delay

As the surface of the copper line corrodes or oxidizes, conduction area in the cross section is reduced, and it can cause the electrical resistance and then RC time delay to increase in the copper interconnect. As mentioned above, the cross-sectional area reduction is a function of time, temperature, activation energy for diffusion of oxidizing agent through the oxidized region and concentration of oxidizing agent. Based on the basic theory of electrical physics, resistance and RC time delay in bare copper line are inversely proportion to the cross-sectional area. Applying constriction current theory to the coated copper interconnects with plating, coating or barrier layers, we find that the increase in resistance and RC time delay during service are due to a localized resistance increase induced by the pits.

A. Bare Copper Line

The general expressions of resistance, R, is

$$R = \rho \int \frac{dl}{S} \tag{14}$$

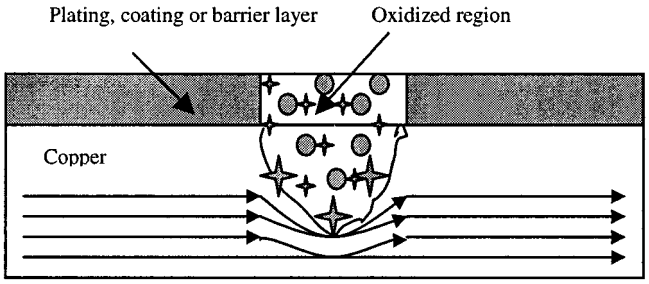


Fig. 4. Lines of current flow and a current constriction.

where ρ is the resistivity of the copper, and dl and S are the length and cross-sectional area of an element of the copper under consideration. When the cross-sectional area of the copper line is a rectangular, the resistance becomes

$$R = \rho\frac{l}{S}. \tag{15}$$

Substituting (7) and (8) into (15), the lifetime resistance is

$$\frac{R(t)}{R(t=0)} = \frac{1}{1 - \frac{2\gamma'}{A_0} D_0^{\frac{1}{2}} t^{\frac{1}{2}} e^{-\frac{Q_a}{2RT_a}}} \tag{16}$$

where $R(t=0)$ is an initial resistance of a copper line and T_a is the absolute temperature of the line under operating conditions. Similarly, the RC time delay for bare copper lines could also be approximately explained in terms of above method as well as geometry factor and space of adjacent lines.

B. Coated Copper Line

When current lines of flow are bent together through narrow areas, resistance increases. This increase in resistance is called the constriction resistance. Fig. 4 schematically illustrates the current flows when a pit grows inward in the coated copper line.

When the conductive cross-sectional area becomes very small compared to nonconductive area, we may apply constriction resistance theory to the pits in the line to estimate the increase in resistance. According to constriction current theory [4], a constriction resistance in a circular conducting area can be expressed as

$$R_c = \frac{\rho}{d} \tag{17}$$

where ρ is the resistivity of conductor and d is the diameter of constriction area.

Following the reasoning used by *Holm* [4] for a noncircular constriction region, in a shape factor of constriction region, the conduction area in the cross section of the constriction region can be approximately expressed as a circular area, in terms of a effective diameter, d_e,

$$S = \frac{1}{4}\pi d_e^2. \tag{18}$$

Substituting (13) into (18), the effective diameter, d_e, has a form

$$d_e = \frac{2}{\sqrt{\pi}}\left[a(A_0 + A_1) - a_0A_1 - \frac{1}{2}\pi\gamma^2 t D_0 e^{-\frac{Q_a}{RT_a}}\right]^{\frac{1}{2}}. \tag{19}$$

We now express the constriction resistance, R_c, by means of d_e,

$$R_c = \frac{\rho f(\gamma)}{\frac{2}{\sqrt{\pi}}\left[a(A_0+A_1) - a_0A_1 - \frac{1}{2}\pi\gamma^2 t D_0 e^{-\frac{Q_a}{RT_a}}\right]^{\frac{1}{2}}}. \tag{20}$$

where $f(\gamma)$ is a form factor which has a value from 0 to 1 and can be determined experimentally.

Thus, substituting the initial conduction area S_0 in (10) into (20), the lifetime constriction resistance, $R(t)$, becomes

$$R_c(t) = \frac{\rho}{\frac{2}{\sqrt{\pi}}\left[S_0 - \frac{1}{2}\pi\gamma^2 t D_0 e^{-\frac{Q_a}{RT_a}}\right]^{\frac{1}{2}}} f(\gamma). \tag{21}$$

Then, the lifetime RC time delay of a coated copper line with a pit, $R(t)$, consists of an initial RC time delay and a RC time delay induced by constriction resistance,

$$R(t)C = R(t=0)C + \frac{\rho C f(\gamma)}{\frac{2}{\sqrt{\pi}}\left[S_0 - \frac{1}{2}\pi\gamma^2 t D_0 e^{-\frac{Q_a}{RT_a}}\right]^{\frac{1}{2}}} \tag{22}$$

where $R(t=0)$ is the initial resistance of line and T_a is the absolute temperature at the constriction region, expressed by following the discussion of *Holm* and *Franz* [4]. The temperature at the constriction region is expected to be higher since there is an additional heat generated in this region. The temperature of the constricted region is given by

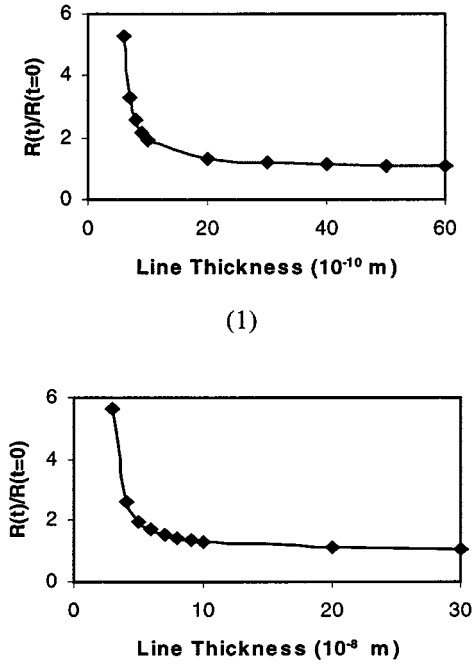
$$T_a = \sqrt{T_0^2 + \frac{U^2}{4L}} \tag{23}$$

where U is the voltage drop across the constriction region, L *Lorenze* constant and T_0 the absolute temperature in the non-constriction region of the coated copper line.

In general, (21) and (22) can be used to estimate a lifetime constriction resistance and lifetime resistance for those copper interconnects with plating, coating and barrier layer when there is only one pit along the line. When there are n pits along the line, an approximate expression of lifetime resistance has the form, assuming that total length of the pits in the line direction is small, compared to the length of the coated copper line,

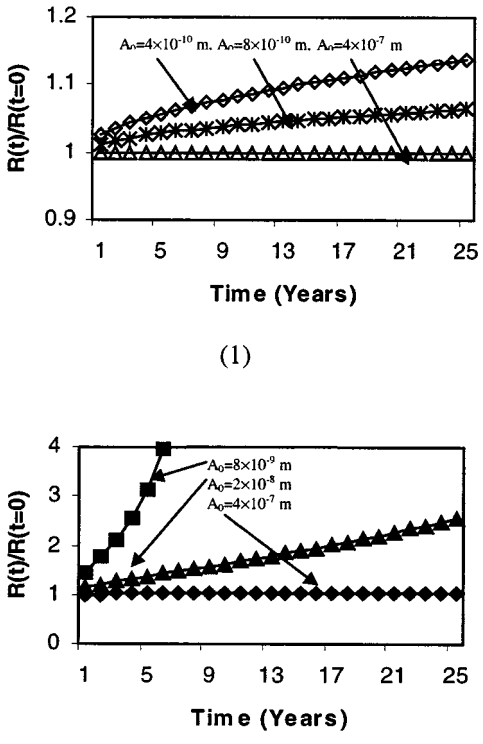
$$R(t)C = R(t=0)C + \frac{\rho C f_1(\gamma)}{\frac{2}{\sqrt{\pi}}\left[S_{0,1} - \frac{1}{2}\pi\gamma^2 t D_0 e^{-\frac{Q_a}{RT_a}}\right]^{\frac{1}{2}}} + \cdots \frac{\rho C f_n(\gamma)}{\frac{2}{\sqrt{\pi}}\left[S_{0,n} - \frac{1}{2}\pi\gamma^2 t D_0 e^{-\frac{Q_a}{RT_a}}\right]^{\frac{1}{2}}} \tag{24}$$

where $S_{0,1}, \ldots, S_{0,n}$ are the initial conduction areas of the copper interconnect and $f_1(\gamma), \ldots, f_n(\gamma)$ are the form factors for those pits along the line.



(1) (2)

Fig. 5. Lifetime resistance increases as the thickness of the copper interconnect is scaled down in $t = 10$ years and (1) $T = 398$ K, and (2) $T = 473$ K.



(1) (2)

Fig. 6. The behavior of lifetime resistance in the copper interconnect thickness for (1) $T = 358$ K, and (2) $T = 448$ K.

IV. Discussion

Analytic solutions of the lifetime resistance of bare copper line on deep submicrometer silicon are presented in Figs. 5–7.

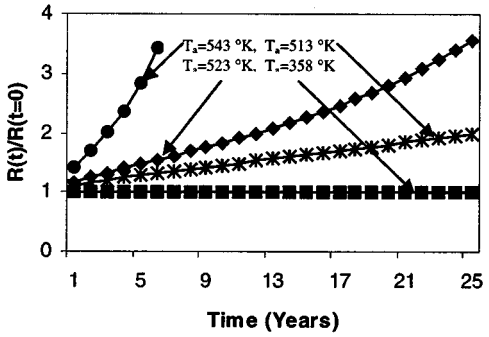


Fig. 7. Lifetime resistance of the copper interconnect for $A_0 = 4 \times 10^{-7}$ m.

TABLE I
TEMPERATURE AND CONCENTRATION DEPENDENCE OF ACTIVATION ENERGY WERE IGNORED IN THE ABOVE ANALYTIC CALCULATION, IN ORDER TO ACHIEVE SIMPLIFICATION

Symbol	Parameter	Value	Dimensions	Ref.
D_0	Frequency factor in copper oxide	6.5×10^{-7}	m^2/s	[9], [10]
R	Gas constant	8.31	J/mole°K	
A_0	Initial height of bare copper line	400×10^{-9}	m	
S_0	Initial area of coated copper line	3.9636×10^{-14}	m^2	
Q_a	Activation energy in copper oxide[1]	1.64×10^{5}	J/mole	[9], [10]
ρ	Resistivity	2.5×10^{-8}	ohm·m	
U	Voltage drop across constriction region	~0.15	V	
L	Lorence constant	2.4×10^{-8}	$(V/°K)^2$	

[1]In order to achieve simplification, temperature and concentration dependence of activation energy were ingored in the above analytic calculation.

Equation (16) and the assumed physical conditions shown in Table I were used to develop the curves.

Fig. 5 clearly indicates the influence of the copper interconnect scale on the lifetime resistance. As the depth of the copper line decreases the resistance increases. As illustrated in Fig. 1 and (16), the lifetime resistance depends strongly on the cross-sectional area of copper interconnect.

Fig. 6 shows the predictions of resistance behaviors of various feature sizes of the copper interconnects during their lifetime at temperatures of 358 K and 448 K. When the feature size of a copper interconnect is scaled down to the nanometer range the lifetime resistance becomes very sensitive to time and temperature. In addition, the lifetime resistance behaviors of the copper interconnects can be observed in Fig. 7. As the temperature in the copper interconnects increases the lifetime resistance goes up significantly and it will impact dramatically device performance, which is one of the most critical concerns in integrated circuits.

Figs. 8–10 represent some of results from (21). Lifetime resistance in the coated copper interconnect, which induces the increase in RC time delay, depends strongly on the applied voltages because of its role in accelerating the growth of oxidizing

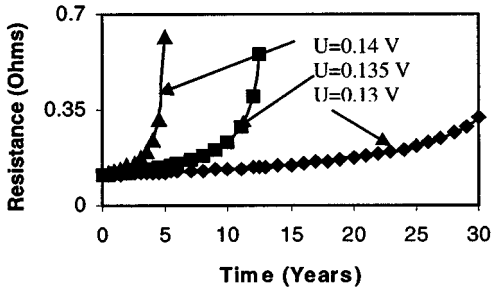


Fig. 8. Lifetime constriction resistance under various applied voltages under initial conductive area $S_0 = 3.9 \times 10^{-14}$ m^2.

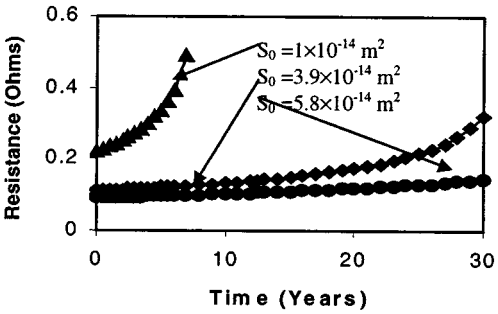


Fig. 9. Lifetime constriction resistance performance as the feature sizes scaled down under $U = 0.13$ V.

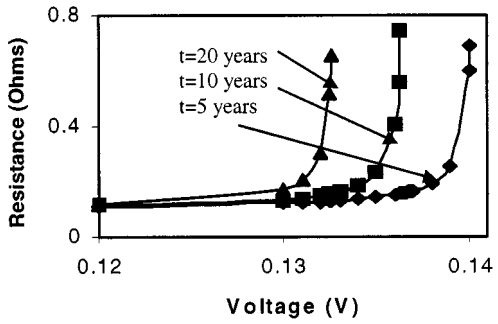


Fig. 10. Effect of applied voltage on the lifetime constriction resistance under $S_0 = 3.9 \times 10^{-14}$ m^2.

region in pits. This situation can be worse as the copper interconnects are scaled down.

In addition to the adverse influence of applied voltages, another undesirable result is that the effect of the feature dimension factor of the copper interconnects on the lifetime constriction resistance becomes more significant as the feature dimension is reduced. Profiles for the copper interconnects in various sizes are presented in Fig. 9. Lifetime constriction resistance versus the applied voltages in the coated copper interconnects is shown in Fig. 10. As voltage increases, the lifetime constriction resistance increases significantly. Fig. 11 illustrates the temperature behavior in pit as voltage increases according to (23).

Similar to the above analytical results, it is possible to obtain, in terms of (22) and (24), more graphical illustrations regarding lifetime RC time delay of the copper interconnects with a single pit, RC time delay induced by constriction resistance and RC time delay of the coated copper interconnects with multiple pits.

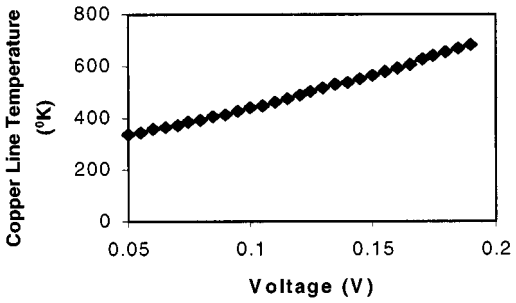


Fig. 11. Line temperature as a function of applied voltage [4].

V. Conclusion

Copper interconnect reliability is a major concern as feature dimension is scaled down. The increase in resistance and RC time delay due to the oxidation or corrosion of copper lines may limit the miniaturization in copper feature dimension unless surface protection from corrosion or oxidation is considered. In this paper we studied some of the main factors responsible for the reliable electrical performance of copper interconnects. The mechanisms of the reduction in conductive area have been investigated to understand the influences of the feature dimensions of copper interconnects, operating conditions, and oxidizing types on the increase of lifetime RC time delay. The present investigation has also developed mathematical models for copper interconnects, which describe the shrinkage behaviors of conductive areas in cross section, characteristics of RC time delay induced by constriction current, and increasing tendencies of lifetime RC time delay under operating environments.

1) The results show that the growth of oxidized region on the bare copper interconnect will result in the increase in lifetime resistance under operating conditions. This increase becomes more serious as the feature dimension of the copper interconnect is scaled down and the operating temperature increases.
2) The increase of lifetime constriction resistance is induced by the pit growth in coated copper interconnects. The impact of this increase in electrical resistance on RC time delay will become significant as the operating voltage increases and the feature dimension of the copper line is scaled down. Surface defects induced during process also play an important role in this increase.
3) RC time delay due to the growth of oxide film or oxidized region at pits will be accelerated by the concentration of oxidizing agent, such as oxygen and operating temperature because of the speed up of diffusion process of oxidizing agent.

Appendix

$$\frac{\partial C}{\partial t} = D_{\mathrm{Cu}} \frac{\partial^2 C}{\partial Z^2}, \quad \text{for } Z' < Z < Z''. \tag{1}$$

Initial boundary conditions, $(t = 0)$ are

$$C = C^{\circ}, \quad \text{for } Z < 0 \tag{2}$$

and

$$C = 0, \quad \text{for } Z > 0. \tag{3}$$

The boundary conditions are at $Z = Z'$, the copper concentration in the oxidized region is in equilibrium with the concentration in the copper,

$$Cz' + 0 = CI, 0 \tag{4}$$

at $Z = Z''$, the copper concentration in phase copper oxide film in equilibrium with the concentration in phase oxidizing agent

$$CZ'' - 0 = CI, I. \tag{5}$$

At the planes of discontinuity, $Z = Z', Z = Z''$, the interfaces between the copper oxide phase and substrate metal and silicon dioxide are displaced by dZ' and dZ'' respectably within time dt, and the amount $[C^{\circ} - CI, 0]\, dZ', [CI, I - 0]\, dZ''$ of copper must be supplied per unit area from the region $Z < Z'$ (copper region), $Z < Z''$ (oxidized region), thus (approximately)

$$[C^{\circ} - C_{I,0}]\, dZ' = D_{\mathrm{Cu}} dt \left(\frac{\partial C}{\partial Z}\right)_{Z'+0} \tag{6}$$

$$C_{I,I}\, dZ'' = -D_{\mathrm{Cu}} dt \left(\frac{\partial C}{\partial Z}\right)_{Z''-0} \tag{7}$$

Following [6], assume tentatively that the plane of discontinuity is shifted proportionally to $\sqrt{t}$, i.e.,

$$Z' = \gamma' 2\sqrt{D_{\mathrm{Cu}} t} \tag{8}$$

$$Z'' = \gamma'' 2\sqrt{D_{\mathrm{Cu}} t} \tag{9}$$

where γ', γ'' are two dimensionless parameters.

A particular solution [6] of (1) is

$$C = A - \mathrm{Berf}\left[\frac{Z}{2\sqrt{D_{\mathrm{Cu}} t}}\right], \quad \text{for } Z' < Z < Z''. \tag{10}$$

By substituting (8)–(10) in (4)–(7), we obtain the equations for γ and γ'

$$\frac{C_{I,0} - C_{I,I}}{C_{I,I}} = \sqrt{\pi}\gamma' \exp(\gamma'^2)[\mathrm{erf}(\gamma') + \mathrm{erf}(\gamma'')] \tag{11}$$

$$\frac{C_{I,0} - C_{I,I}}{C^{\circ} - C_{I,0}} = \sqrt{\pi}\gamma'' \exp(\gamma''^2)[\mathrm{erf}(\gamma') + \mathrm{erf}(\gamma'')] \tag{12}$$

which may be solved graphically or numerically if $C^{\circ}, CI, 0$ and CI, I are given. The diffusion coefficient D_{Cu} can be determined from the observed rate of displacement of the boundaries by means of (8) and (9)

$$D_{\mathrm{Cu}} = \frac{(Z')^2}{4\gamma' t}$$

and

$$D_{\mathrm{Cu}} = \frac{(Z'')^2}{4\gamma'' t}. \tag{13}$$

Similar to the above analysis, we can have another one dimensional diffusion equation for oxidizing agent, such as oxygen. Therefore, the boundary growth inward can also be expressed as (14) after performing the same procedure as above,

$$Z' = 2\gamma'\sqrt{Dt} \tag{14}$$

where

$$D = D_0 e^{-\frac{Q_a}{RT_a}} \tag{15}$$

where D_0 is the frequency factor for the oxidizing agent, Q_a the activation energy of oxidizing agent through the copper oxide product, and R universal gas constant. T_a is the absolute temperature of the oxidized region.

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Electronic parts obsolescence is a serious problem causing many millions of dollars to be expended annually on recovery actions and seriously compromising the long-term sustainability of systems. While technological advances continue to fuel product development, engineering decisions about how and when to use a new part or technology and the trade-offs of associated risks and benefits differentiate the winning from the losing products.

This book presents a methodology to forecast the years to obsolescence and the life cycle stages of electronic parts using part sales and technology trend data. The book also presents the underlying reasons for part obsolescence and a wide variety of tactics and strategies that can be deployed by the part user to mitigate the effects. This enables engineers to better manage the part selection and management process for their systems and reduce costs.

The predictions derived from the models allow engineers to effectively manage the introduction and on-going use of electronic products based on the projected life cycle of the parts incorporated. Examples of the application of the methodology to various part types is discussed and obsolescence predictions are demonstrated using commercially available sales data. The use of this methodology can significantly reduce design iterations, inventory expenses, sustainment costs and overall life cycle costs.

This book will also be of interest to marketing and business development managers, contract negotiators, proposal writers and logistics support personnel.

PREFACE

This book reviews life-cycle stages and presents a methodology for forecasting the years to obsolescence for electronic parts. The prediction of obsolescence enables engineers to more effectively manage the introduction and on-going sustainment of long field-life products based on the projected life-cycle of the parts. The obsolescence prediction methodology is a critical element within risk-informed parts selection and management processes. Engineers must be aware of the part life-cycles, otherwise, an engineer can end up with a product, whose parts are not available, which cannot perform as intended, cannot be assembled and cannot be maintained without high life-cycle costs. While technological advances continue to fuel product development, engineering decisions regarding when and how a new part will be used and the associated risks traded-off with a new part and technology, differentiates the winning from the losing products.

Obsolescence of electronic parts is a major contributor to the life-cycle cost of low-volume complex electronic systems and long field-life systems such as avionics. Technology in 21st century electronic manufacturing is being driven by computers. Obsolescence can be considered a universal concern for both the high-volume industries that drive technology development and the low-volume industries that depend on this technology.

So how does obsolescence matter to the high-volume industries? Volume of manufacture in the high-volume industries is high. It is important to ensure that the system manufacturer has a continuous supply of parts throughout the manufacturing period of the system. Lead times matter in the high-volume industry as time-to-market is critical to stay afloat amidst stiff competition. Discontinuance of part supply due to part obsolescence would lead to heavy losses and some form of redesign will be required after determining the right substitute. Usually the part manufacturer provides a part discontinuance notice and a recommended substitute part. Hence, the degree of concern due to obsolescence in the high-volume industry is restricted to the downtime when a certain part is not avail-able.

In the case of the low-volume industries, the case is different; parts specific to the low-volume industry are not as widely available as parts used by the high-volume industry. Industries such as avionics are being forced to migrate to commercial grade parts, which raises issues such as life-cycle mismatches. With life-cycles of commercial parts around 18 months, the life-cycle mismatch between commercial parts and ‘long life’ low-volume systems is very high, leading to the problem of obsolescence.

In developing an effective plan to combat component obsolescence, understanding the nature of the problem is critical. There are, essentially, three types of obsolescence.

The first type of obsolescence is due to technological evolution. A new generation of technology effectively makes its predecessor obsolete. An example of this would be faster microprocessors making the slower ones obsolete. Typically, the new generation technology has improved performance and functionality, often at lower cost than its predecessors.

The second type of obsolescence is caused by technological revolution where a new technology supersedes its predecessor. An example of this is the Fiber Distributed Data Interface (FDDI) that is becoming obsolete as the market moves towards adopting Fiber Channel as the communications technology of choice.

The third type of obsolescence caused by market forces. This is caused when the demand for a component or technology falls and the manufacturer considers it uneconomic to continue production. This is an increasing problem, as the low-volume market no longer commands the

purchasing power necessary to persuade manufacturers to continue production; part manufacturers and distributors may not be willing to manufacture or stock parts that have a small market. The cost of managing distribution of low-volume parts while providing affordable prices is a challenge and hence the few distributors that do provide low-volume parts are expensive.

This book presents a methodology to forecast life-cycles of electronic parts, in which both years to obsolescence and life-cycle stages are predicted. The methodology embeds both market and technology factors based on the dynamic assessment of sales data. The predictions enabled from the models developed al-low engineers to effectively manage the introduction and on-going use of long field-life products based on the projected life-cycle of the parts incorporated into the products. Application of the methodology to various part types is discussed and obsolescence predictions are demonstrated. The goal is to significantly re-duce design iterations, inventory expenses, sustainment costs and overall life-cycle product costs.

Who This Book Is For

This book enables the manufacturers of high and low-end products to manage obsolescence of parts that are used in their systems. High-volume manufacturers include computers, cell phones and electronic entertainment systems. Low-volume manufactures include avionics, automotive, space, medical, defense and oil drilling. Engineers must be aware of the part life-cycles, otherwise, an engineer can end up with a product, whose parts are not available, which cannot per-form as intended, cannot be assembled and cannot be maintained without high life-cycle costs. While technological advances continue to fuel product development, engineering decisions regarding when and how a new part will be used and the associated risks traded-off with a new part and technology, differentiates the winning from the losing products. This book is intended for engineers and managers involved in the design of low-volume complex electronic products. Members of product teams, marketing professionals, business development professionals, contract negotiators and proposal writers, will also find the guidance provided in this book particularly useful.

What This Guidebook Contains

This guidebook explains the life-cycle of an electronic part and presents a process for life-cycle forecasting of parts used in an electronic system based on sales data, with case studies illustrating the method, then obsolescence management strategies are explained.

Chapter 1 describes electronic part life-cycle as it progresses from design and introduction through to obsolescence and final phaseout. The six stages of an electronic part life-cycle are explained and the changes that are undergone by attributes such as sales, price, usage, part modification, number of competitors and profit margin are presented.

Chapter 2 describes the change management methods and controls commonly used by semiconductor manufacturers and the types of change that they make. Relevant standards and guides are introduced and described. Some of the major change management standards development bodies are discussed and examples are given to provide the reader with information on the nature of information that is covered.

Chapter 3 explains a methodology for predicting obsolescence based on an analysis of readily available part sales data. After identifying the part and technology group and the primary and secondary attributes that affect the life of the electronic part, sales curves based on a Gaussian model are used to predict the life-cycle and the time to obsolescence of the part. Existing methods to predict electronic part obsolescence such as the TACTech method of life-cycle forecasting is explained as an example.

Chapter 4 illustrates the application of the sales data based life-cycle forecasting methodology in the form of case studies on seven part types. The part types are DRAMs, SRAMs, ROMs and flash memory, microprocessors, microcontrollers, logic, analog and ASICs. For each of these part types the detailed information on the part type, market trends, life-cycle of the part type and the zone of obsolescence is presented.

Chapter 5 explains the various strategies that can be employed by equipment manufacturers to combat the problem of obsolescence. The strategies presented are a combination of long term and short term strategies. The pros and cons of the strategies are explained. The chapter also addresses economic factors and provides a guide to select an obsolescence management strategy. Some of the major obsolescence management guidance documents developed by industry is described.

Appendix A provides, in summary form, the constants for each of the part types considered in the book.

Finally, an extensive list of references is provided to aid the reader in finding additional information.

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